Multi-Stage GaN Power Amplifier Reference Design - Delivering 150 W for 3.1 - 3.5 GHz S-Band Radar

Introduction

MACOM developed a three-stage application circuit demonstrator using two 50 V GaN products. The two products are a QFN 2 stage plastic MMIC used as a driver (CMPA2735015S) and an input matched metal ceramic packaged HEMT transistor (CGHV35120F). The purpose of this application circuit is to demonstrate MACOM GaN HEMT technology capabilities with respect to harmonic content, power added efficiency (PAE), size weight and power (SWaP). The prototype was evaluated using a 10% duty cycle pulsed single tone signal with a 100 µs pulse width. This application note describes the typical performance that has been achieved and that which can be expected when evaluating the demonstrator. Details of the circuit are included for further understanding of the topology.

Features

- 400 MHz Instantaneous Bandwidth
- 48 dB Small-Signal Gain
- 42 dB Associated Power Gain (up to 150 W output power)
- 63% Power Added Efficiency at 150 W average power (3.1 to 3.5 GHz)
- -46 dBc worst case Harmonic content (H2 through H4) at up to peak Efficiency
- Minimum Physical Size: 0.9 x 2.2 in (23 x 56 mm)

Application Note

Typical Demonstrator Performance - CGHV35120F-AMP2

Parameter	Units	Frequency (GHz)				
		3.1	3.2	3.3	3.4	3.5
Small Signal Gain	dB	50.0	49.3	48.5	4739	47.4
Power Gain	dB	42.4	42.3	42.2	42.3	42.3
Power Out	dBm	52.5	52.3	52.2	52.2	52.3
Power Added Efficiency	%	68.4	67.0	65	63.6	64
Harmonizing Level, (worst case)	dBc	-47	-52	-45	-47	-46

Schematic: CGHV35120F-AMP2 Demonstration Circuit

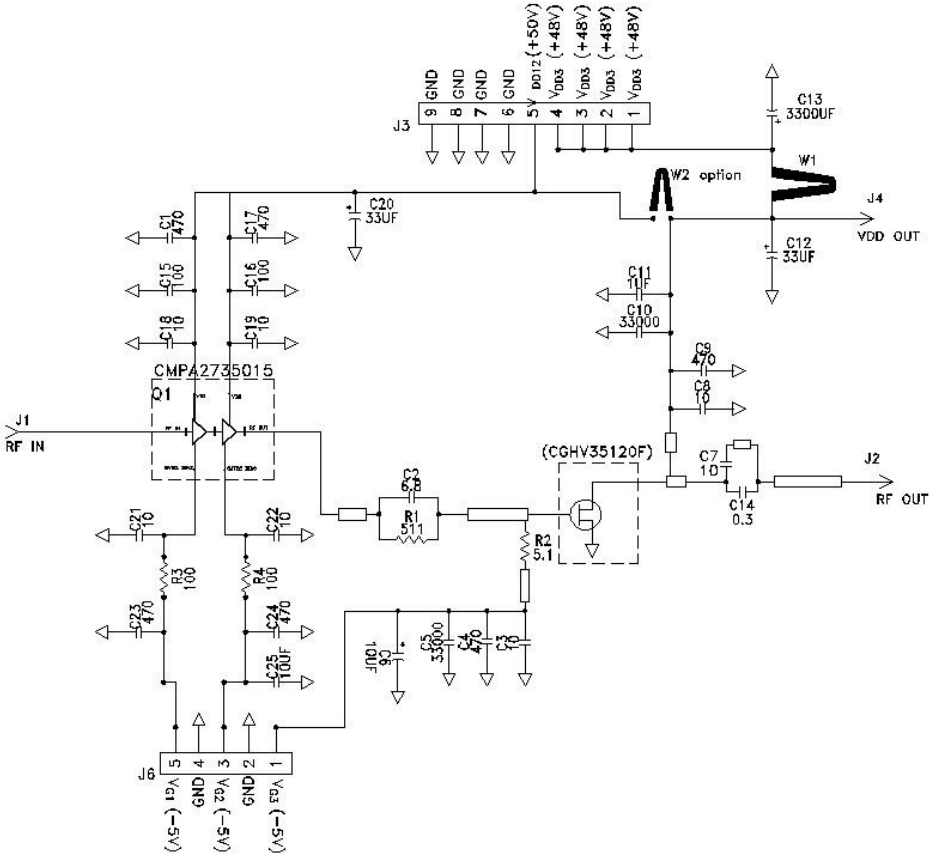

Figure 1: Schematic of CGHV35120F-AMP2 Demonstrator Circuit

Printed Circuit Board: CGHV35120F-AMP2 Demonstration Circuit

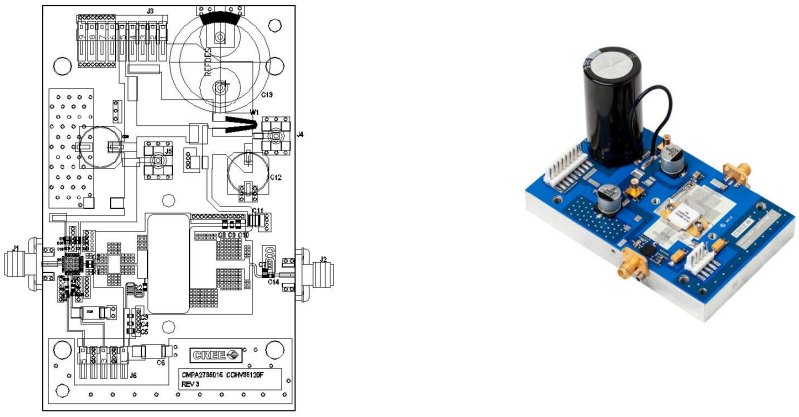

Figure 2. CGHV35120F-AMP2 Demonstrator Printed Circuit Board Assembly

Application Note

Typical Performance of the CGHV35120F-AMP2 Demonstrator

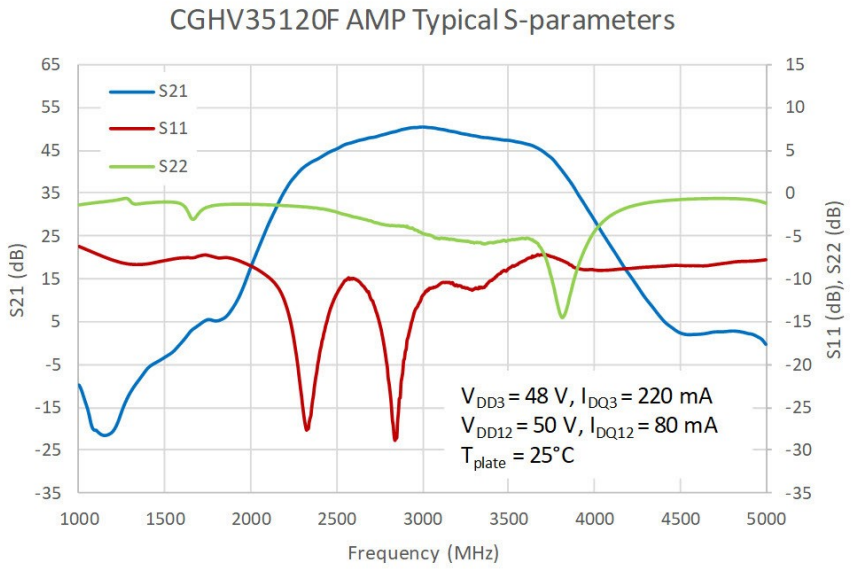

Figure 3. Typical S-Parameters

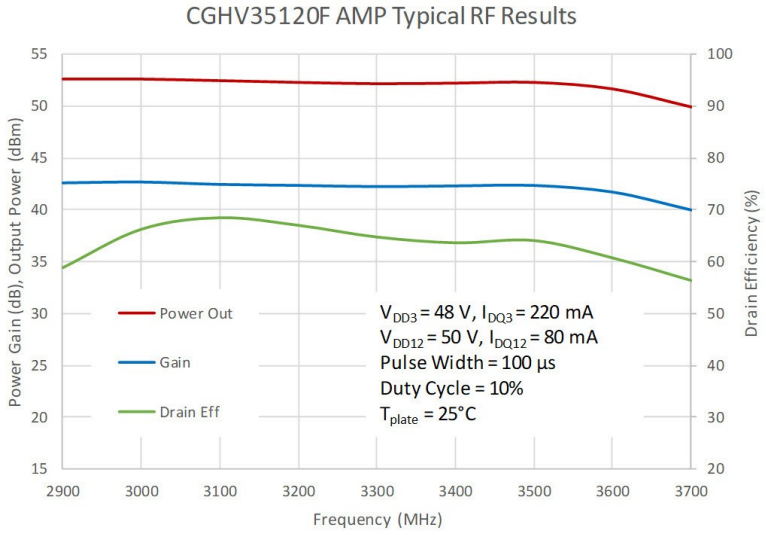

Figure 4. Typical Power Gain, Efficiency and Output Power vs. Frequency

Application Note

CGHV35120F-AMP2 Demonstrator Bill of Materials

Reference Designator	Description (type, value, rating(s), size	Qty.	UOM
C1, C4, C9, C17, C23, C24	CAP, 470PF, 5%, 100V, 0603, X7R	1	Each
C2	CAP, 6.8pF, +/- 0.25 pF,250V, 0603, ATC	1	Each
C3	CAP, 10.0pF, +/-5%, 250V, 0603, ATC	1	Each
C5, C10	CAP, 33000PF, 0805, 100V, X7R	2	Each
C6, C25	CAP 10UF 16V TANTALUM	1	Each
C7	Capacitor, ATC, 10pF, +/- 5%, 55x55mils (Case A)	1	Each
C8	CAP, 10pF, +/- 1%, 250V, 0805, ATC	1	Each
C11	CAP, 1.0UF, 100V, 10%, X7R, 1210	1	Each
C12, C20	CAP, 33 UF, 20%, G CASE	1	Each
C13	CAP, 3300 UF, +/-20%, 100V, ELECTROLYTIC	1	Each
C14	CAP, ATC100A, 0.3pF, +/-0.1pF, 55x55mils (CASE A)	1	Each
C15, C16	CAP, 100pF, 5%, 0603, ATC	2	Each
C18, C19, C21, C22	CAP, 10.0pF, 5%, 0402, ATC	4	Each
J1, J2	CONN, SMA, PANEL MOUNT JACK, FLANGE, 4-HOLE, BLUNT POST, 20MIL	2	Each
J3	HEADER RT>PLZ .1CEN LK 9POS	1	Each
J4, J5	CONNECTOR; SMB, Straight, JACK, SMD	1	Each
J6	HEADER RT>PLZ .1CEN LK 5POS	1	Each
R1	RES, 511 OHMS, +/- 1%, 1/16W,0603	1	Each
R2	RES, 5.1, OHM, +/- 1%, 1/16W,0603	1	Each
R3, R4	RES, 100, OHM, +/- 1%, 1/16W, 0603	1	Each
Q1	Transistor CMPA2735015S	1	Each
W1	CABLE, 18 AWG, 4.2	1	Each
	PCB, RO4350, 10 MIL THK, CGHV35120F	1	Each
	BASEPLATE, AL, 4.0 X 2.5X 0.5	1	Each
	2-56 SOC HD SCREW 1/4 SS	4	Each
	#2 SPLIT LOCKWASHER SS	4	Each

Conclusion

This application note has given a summary of the CGHV35120F AMP application reference design and measured results of the amplifier employing MACOM 5x5 QFN CMPA2735015S and metal ceramic package CGHV35120F GaN HEMT devices. The design provided an amplifier with power gain greater than 42 dB over a 400 MHz bandwidth centered at 3.3 GHz, resulting in worst case output referred harmonic level of -46 dBc, average output power of 150 W at a drain efficiency of 63%. This performance is achieved in a fixture size of roughly 0.9 x 2.2 inches.

CGHV35120F WITH DRIVER (CMPA2735015S) TEST FIXTURE SETUP INSTRUCTIONS FOR TEST FIXTURE, PART NUMBER AD-838303-AMP_2

1. Position the test fixture such that the RF in J1 (50 Ω) is connected to the left side of the fixture and the RF out J2 (50 Ω) is connected to right side of the fixture.
2. Jumper wire W2 (Ties Drains 1, 2 and 3) is **not** in place. Drains 1 and 2 will be separated from Drain 3.
3. Connect the 9 (J3) and 5 (J6) pin bias cable to both the top and bottom connector.
4. Verify all power supplies are at 0 volts before turning on.
5. Connect the J3 **YELLOW** wire (pin 5) to first drain power supply. Connect the test fixture J3 **RED** wires (pins1,2,3,4) from the **TOP** connector to the second drain power supply.
6. Connect the test fixture J6 **YELLOW** wires (pins 3 and 5) from the **BOTTOM** connector to the CMPA2735015S gate **control** power supply “1”.
7. Connect the test fixture J6 YELLOW wires (pin 1) from the BOTTOM connector to the CGHV35120F gate control power supply “2”.
8. Connect the test fixture **BLACK** wires to the return (common) terminals of the gate and drain power supplies.
9. Verify connections with the test fixture schematic on the data sheet.
10. Adjust the Gate power supplies to -5V. Turn on the gate bias power supply.
11. Turn on the two drain bias power supplies. Adjust the first power supply to +50 volts and the second supply to +48V. There should be **NO** current flow from the power supplies.
12. Ensure RF drive power is “OFF”.
13. Set Idq for Driver: Ensure Gate Supply “1” is set to -5v. Adjust the Driver Idq current by changing the Gate bias supply “1” for a drain current (Idq) of 80 mA. Record gate voltage (Vg of driver).
14. Set Idq for Flange Device: Ensure Gate Supply “2” is set to -5 v. Adjust the flange device Idq current by changing the Gate bias supply “2” for a drain current (Idq) of 220 mA. Record gate voltage (Vg of Flange device).
15. Apply low RF drive, 0dBm (3.1- 3.5 GHz or frequency of application circuit), and verify the fixture has approximately 45dB of gain. Increase RF drive to the desired output level and verify the performance with the transistor data sheet. Do not apply more than 13 dBm input power.
16. **To shut down the circuit:** Turn off the RF test signal. Turn off the +50 V Drain supply and lastly turn off the gate voltage supplies.

Application Note

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